SRC5986E RUGGED MICRO-TRANSCEIVER

A **small form factor multi-channel software defined radio frequency (RF) system** for commercial and government spectrum applications

APPLICATIONS

- Designed for stand-alone missions or integrated as a sub-system component
- REDHAWK FEI 2.0 Compliant Device

SPECIFICATIONS

Size, Weight and Power Specifications

- Input range: 7V to 15V, nominal 12V
- Backup battery support (CR-123A)
- Typical power consumption: 30W
- Dimensions: 11.2in x 3.44in x 3.33in
- Weight: 4.65 lb
- Operating temperature: -40 to 65°C
- Environment: Designed to meet MIL-STD-810

Transceiver RF Specifications

- Tuning range: 70 MHz – 6 GHz
- Tuning step-size: < 3 Hz
- RF channel bandwidth: 200 kHz to 112 MHz
- Typical I/Q balance: > 50 dB
- A/D converter sample rate: 233 Ksamples/sec to 61.44 Msamples/sec
- A/D converter sample width: 12 bits
- RF I/O: SMA (50 ohms)
- Number of RF transceivers: 4 (independently configurable to receive or transmit)
- Receive input: internal limiters allow up to 2W (+33 dBm) survival
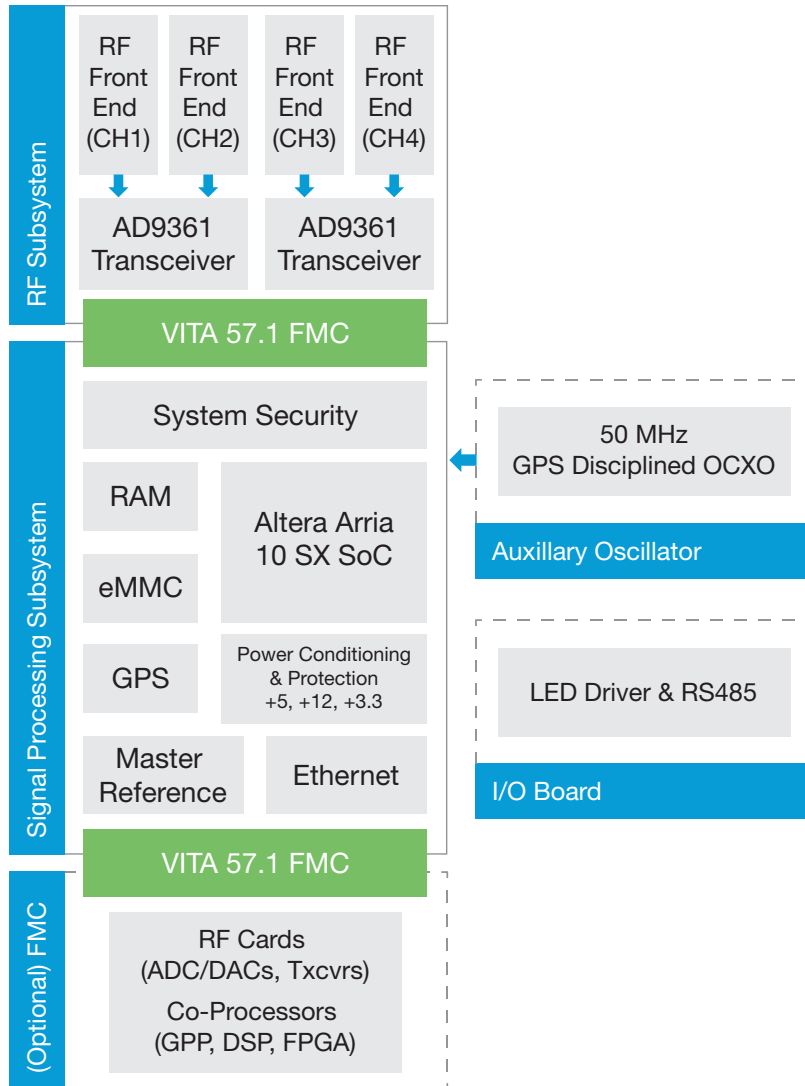- Transmit output: ≥ 0 dBm up to 6 GHz

- Tuning time: < 50 us
- Pre-select filter bank: 11 internal sub octave filter paths
- Typical noise figure: 8.5 dB [LNA], 22 dB [BYP] (2.4 GHz estimate used)
- Typical IIP3: -20 dB [LNA], -5 dB [BYP] (2.4 GHz estimate used)
- Gain control: 0 to 96 dB (0 to 76 from AD9361 with bypassable amplifier > 20 dB)

Digital Specifications

- SoC: Altera Arria 10 SX 660 (Dual-Core ARM Cortex A9)
- MCU: Freescale Kinetis K65 MCU (ARM Cortex-M4F) for health and security monitoring
- RAM: 2GB DDR3L-1600 SDRAM with ECC
- Internal flash storage: 64GB eMMC for Linux and root filesystem
- Operating System: Linux Kernel 4.9
  - One 10 gigabit ethernet (10GBASE-SR) through MIL circular connector
  - Dedicated RS-232 UARTs to MCU and SoC
  - 1000BASE-T ethernet for command and control

- IQ Streaming using VITA 49.0 over UDP
- USB
  - USB to UART bridge allows console access to MCU and SoC
  - USB mass storage device interface
  - USB headphone/microphone accessory interface
- Integrated GNSS/GPS receiver with 1PPS for disciplining internal OCXO
  - Optional integrated SAASM device in SRC5986B variant

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RF Subsystem

RF Front End (CH1)	RF Front End (CH2)	RF Front End (CH3)	RF Front End (CH4)

AD9361 Transceiver	AD9361 Transceiver

VITA 57.1 FMC

Signal Processing Subsystem

System Security

RAM

eMMC

GPS

Altera Arria 10 SX SoC

Power Conditioning & Protection +5, +12, +3.3

Master Reference

Ethernet

VITA 57.1 FMC

Auxillary Oscillator

50 MHz GPS Disciplined OCXO

I/O Board

LED Driver & RS485

(Optional) FMC

RF Cards (ADC/DACs, Txcvrs)

Co-Processors (GPP, DSP, FPGA)

J20

STAT 1
STAT 2
J4-RF4
J3-RF3
J2-RF2
J1-RF1

FEATURES

- **Base-Mezzanine Architecture**
  - Internal auxiliary 50 MHz OCXO
  - Common baseband processor card
  - 2x VITA 57.1 FMC expansion sites

- **Baseband Processor Card**
  - 1.5 TFlop Altera Arria 10 SoC
  - Multiple console access via microUSB port
  - High speed RAM and flash access
  - Ultra-low power MCU for health and security monitoring

- **RF Mezzanine**
  - Four RF receive paths (configurable as two separately tunable phase coherent pairs, or four phase coherent channels, using a single LO)
  - 11 selectable sub-octave filters per RF channel
  - 70 – 6000 MHz up to 112 MHz IBW
  - Noise figure 5 dB (50 MHz) to 15 dB (6 GHz)
  - 2W limiter
  - RF loopback for finite calibration of entire signal chain

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